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Radiation Testing, Characterization and Qualification Challenges for Modern Microelectronics and Photonics Devices and Technologies

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Abstract: *At GOMAC 2007, we discussed a selection of the challenges for radiation testing of modern semiconductor devices focusing on state-of-the-art memory technologies. This included FLASH non-volatile memories (NVMs) and synchronous dynamic random access memories (SDRAMs) [1].*

In this presentation, we extend this discussion in device packaging and complexity as well as single event upset (SEU) mechanisms using several technology areas as examples including: system-on-a-chip (SOC) devices and photonic or fiber optic systems. The underlying goal is intended to provoke thought for understanding the limitations and interpretation of radiation testing results.

Keywords: CMOS; radiation effects; digital electronics; photonics.

Introduction

Radiation effects testing, in general, has become more challenging [2]. In particular, testability of devices for single event effects (SEE) is struggling with multiple considerations including:

- Complex packaging related challenges that include accessibility by the ground-based particle to the die (required for heavy ion SEE testing), thermal heating and cooling for worst-case testing, and shadowing by the package during angular testing (i.e., the package being in the way of the beam when the beam is not coming perpendicular to the die),
- Questions concerning direct ionization potential of scaled complementary metal oxide semiconductor (CMOS) technologies and photonic devices driving choices for test energy selection and space upset rate prediction methods, and,
- Design complexity internal to devices such as hidden registers, test modes, and application-specific usage impacting fault isolation, test data collection and interpretation.

In this talk, we shall consider these changes above as they pertain to radiation effects testing of modern commercial SOC and photonic devices in the natural space environment. In particular, the emphasis will be on heavy ion and proton SEE testing with a lesser emphasis on total ionizing dose (TID) evaluation. The environments specific to the military radiation environment such as prompt dose and neutron are considered out-of-scope for this presentation.

The approach will be to discuss each of the three areas just delineated. This will include several examples of specific devices or technologies illustrating these challenges for radiation testing. This should be viewed as a snapshot of issues and not a comprehensive detailed analysis.

Complex Packaging as Related to SEE Testing

As integrated circuit (IC) packaging has evolved alongside the scaling of CMOS semiconductor technology, testability-related challenges have come to the forefront for heavy ion SEE testing. This stems from a relatively straight-forward fact: the typical heavy ion ground test sites utilize ion energies not equivalent to those existing in space. Space energy regimes easily penetrate packaged devices (as well as spacecraft) requiring a strong magnetic field to provide protection. Ground-based facilities, with the exception of a few sites that are difficult to obtain access, do not have this type of energy/penetration capability. Figure 1 illustrates this condition showing the typical accelerator ion (low energy) versus the space (high energy) in penetrating a device package to the die.

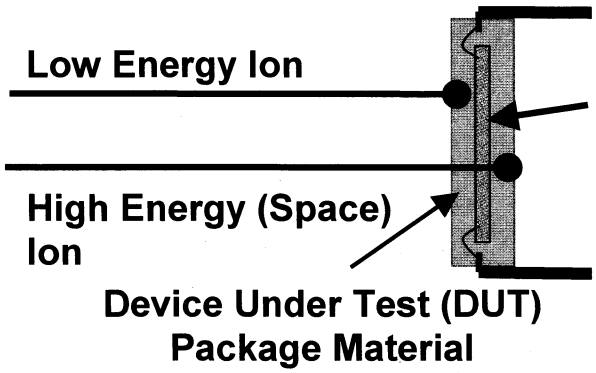

Figure 1. Penetration Difference between Space and Ground Heavy Ions

This limited penetration range thus requires the removal of all (delidding) or some (thinning) of the package material. In [1], we discussed some of the challenges related to this deprocessing requirement. For complex SOCs, for example, the packaging might be a flip-chip in a Ball Grid Array (BGA). The die, in this case, would face the bottom-

side of the package (i.e., the balls). Ground accelerator heavy ions thus would require ion access from the package topside usually after thinning the silicon providing the particle entry via the die backside.

Continuing with this same package, many higher performing silicon devices such as microprocessors require a means of cooling the devices for thermal considerations. The cooling system is usually mounted on this same package topside that we would require access to for the particle beam. Figure 2 shows one such top-mounted fan designed for processor usage. Clearly, if a particle has difficulties penetrating a device's package, ion access through this type of assembly would be impossible. Hence, alternate cooling methods must be sought (especially considering that some of the ground facilities require testing in a vacuum ruling out air cooling). In addition cooling (or when required, heating) from the package bottom is equally difficult (the balls attaching to the test fixture are in the way). Placing heaters/coolers around the package and monitoring via infrared temperature is one approach, but can limit the temperature range for testing (i.e., may not be able to test at high end of mil-temp range, for example).

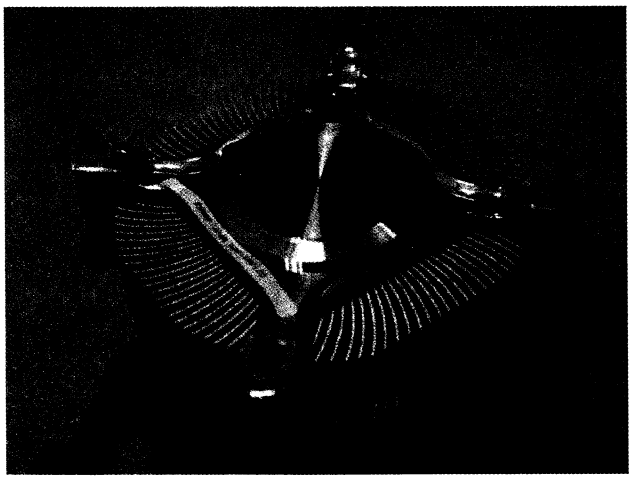

Figure 2. Typical Processor Fan Assembly

The last packaging concern discussed herein is beam incidence angles. If the particle beam is directionally coming perpendicular to die (i.e., straight into the die surface), the above discussions are still valid. However, many device technologies require testing at multiple angles of incidence with the DUT being tilted in relation to the beam in multiple axes (i.e., pitch, roll, yaw) in order to investigate asymmetry as well as effects of a single ion affecting multiple sensitive sites within a die. Package material, heating, cooling, and monitoring systems must all be taken into account when determining available test angles. Figure 3 shows an example for silicon on insulator (SOI) technology and the effects from proton particle incidence angle. Asymmetric effects have also been observed on multiple devices showing differences on angular response from opposing angles (e.g., +/- 45 degrees or after a 90 degree DUT rotation). Packaging issues, as noted, exacerbate the test difficulties in providing many angular datasets. While modeling can be an aid, when testing is performed on a strictly commercial device with unknown cell/transistor layouts and circuit designs, it is problematic to predict omnidirectional responses.

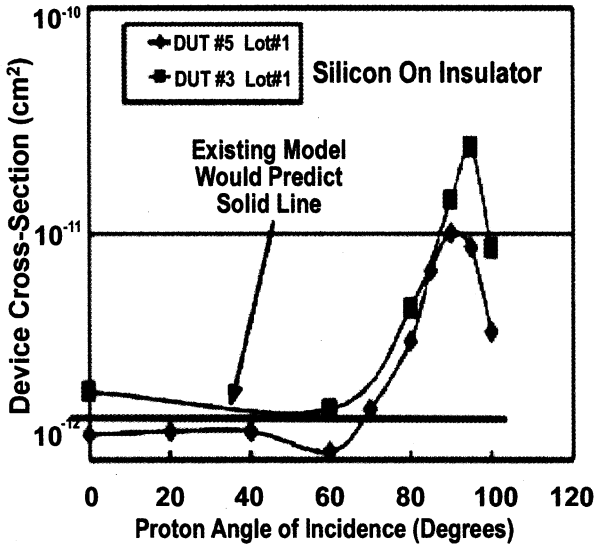

Figure 3. Angular Incidence Effects for Protons on SOI [3]

SEU Sensitive Technologies; Proton Test Energies and Space Event Rate Prediction

As the critical charge required for causing an upset has decreased with scaled CMOS feature sizes and dwindling power supply voltages, the concern over the SEU mechanism(s) caused by an energetic proton interaction has become a consideration. With older CMOS feature sizes, say greater than 90nm, a proton interaction would cause an SEU via a nuclear reaction inside the silicon. This is indirect ionization. The energy that was deposited directly by the proton during its transit through the device was insufficient to cause such an effect. Now with CMOS scaling, this may not be the case.

Photonic devices such as optocouplers or optical detectors are known for potentially being direct ion sensitive and SEUs could be caused by both direct and indirect ionization via protons. Figure 4 is an example of proton single event transient (SET) data on an optocoupler showing energy and angular effects [4]. The characteristic of the indirect ionization events is a relatively flat response with energy and angle. The angular increase at grazing angle (along the plane of the detector diode) as well as the energy response indicate that direct ionization mechanisms are at play as well (note that lower proton energies deposit greater energy per unit pathlength than higher proton energies). Traditional space rate prediction tools such as CREME96 are not equipped to handle this mixed mode of mechanisms. Details can be found in [5].

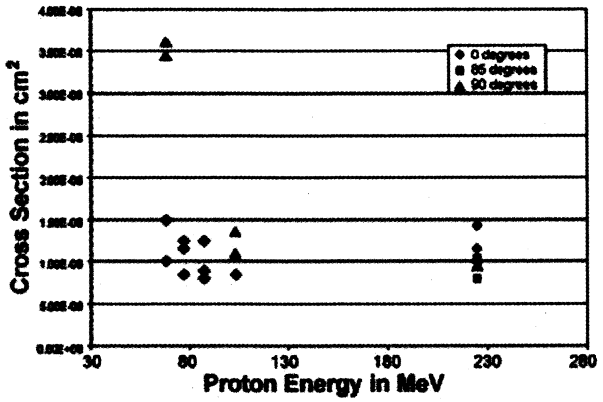

Figure 4. Proton SET Data on a Optocoupler

Recent data has shown that modern CMOS technology semiconductors may now be susceptible to direct ionization from protons as well. From the test perspective, this impacts the choice of energies required for a proton SEU test expanding the number of energies required as a minimum. In addition, the standard SEU space rate prediction tools are ill-suited for this mixed issue and new methods are being developed [see for example 7]. This direct ionization potential for CMOS devices is an area undergoing much research at this time.

Internal Device Complexity and Radiation Testing

SOC devices are by their nature extremely complex internally. Take, for example, a field programmable gate array (FPGA). Figure 5 shows the basic architecture of an FPGA. From this perspective, it looks simply like a piece of silicon where you can program how logic is interconnected. This is the "old school" concept. State-of-the-art FPGAs are vastly more complex with powerful intellectual property (IP) such as embedded processors, digital signal processors (DSPs), gigabit per second I/O links, and much more. These IP can be hard (fixed silicon) or soft (user-embedded) and most users will end up with a mix of IP and logic designs. Now consider a FPGA with embedded processors. Not only can a designer program the hardware configuration, they can also program the software.

This user-definable SOC, while a boon to many for its features, is a research project unto itself to radiation test. In some cases, FPGAs are reconfigurable and use SRAM-like storage cells for its configuration. Considering one of these style of FPGAs with embedded processors provides a myriad of potential types of SEUs that can occur including: change of configuration memory, state machine errors, logic errors related to cell spacing (multi-bit upsets or MBUs) or operating speed (SEU event may last longer than one clock period), software interrupts, and more.

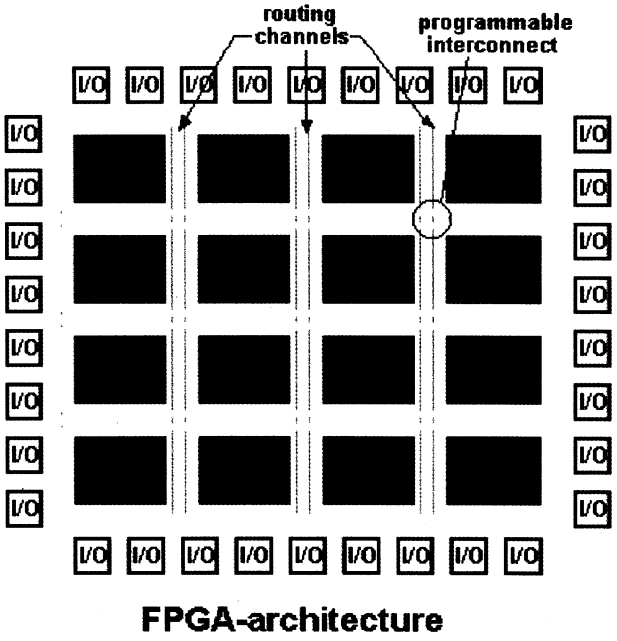

Figure 5. Generic FPGA Architecture

Many issues follow from this type of device complexity. Some of these issues are:

- Fault isolation: understanding what within the device is causing an event. The current SEE test facilities are ill-equipped for this purpose and higher energy microbeam facilities where you can focus a particle to a small spot size to identify what is upsetting as well as penetrating through layers of silicon would be advantageous. Other tools, such as two photon absorption (TPA) layers may also be useful [8, for example]. Of course, these SOCs are usually in packages such as BGAs that are flip-chip and the challenges discussed earlier play into this discussion as well.
- Data interpretation: with the vast array of user configurability, operating modes, speed of operation, and so forth, it is impossible to cover all the bases for each potential application of the device. What this implies is that most test data is suspect when trying to relate to a differing application.
- Statistical data gathering: in many FPGAs, the susceptibility of the configuration storage memory may be the "big particle target" overshadowing physically smaller and/or less susceptible portions of the device. What may happen is that SEUs may occur during a test in these "smaller" circuit portions, but are lost when the "bigger" area is upset. And
- TID parametric tests: given the speed, logic size, IP, etc. in these devices, trying to reproduce the manufacturers detailed test vectors and parametric measurements would require years and years of

effort as well as millions of dollars. Simplified tests are often undertaken looking primarily at functional go/no-go and limited parameters. These data must be viewed in the limited regard in which they were taken. Working with the device manufacturer and using their test system should be considered for these complex devices.

Discussion

We have discussed just a few of the emerging challenges related to modern radiation effects testing. These are just the tip of the iceberg and should not be viewed as a comprehensive discussion. The final thought is that radiation data must be very carefully scrutinized to understand what the data does or does not contain. In addition, the application-specific orientation of radiation data continues to grow.

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